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Fault self-repair strategy based on evolvable hardware and reparation balance technology



Zhang Junbin, Cai Jinyan ^{*}, Meng Yafeng, Meng Tianzhen

Department of Electronic and Optical Engineering, Mechanical Engineering College, Shijiazhuang 050003, China

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swarm optimization;
Reparation balance
technology

Abstract In the face of harsh natural environment applications such as earth-orbiting and deep space satellites, underwater sea vehicles, strong electromagnetic interference and temperature stress, the circuits faults appear easily. Circuit faults will inevitably lead to serious losses of availability or impeded mission success without self-repair over the mission duration. Traditional fault-repair methods based on redundant fault-tolerant technique are straightforward to implement, yet their area, power and weight cost can be excessive. Moreover they utilize all plug-in or component level circuits to realize redundant backup, such that their applicability is limited. Hence, a novel self-repair technology based on evolvable hardware (EHW) and reparation balance technology (RBT) is proposed. Its cost is low, and fault self-repair of various circuits and devices can be realized through dynamic configuration. Making full use of the fault signals, correcting circuit can be found through EHW technique to realize the balance and compensation of the fault output-signals. In this paper, the self-repair model was analyzed which based on EHW and RBT technique, the specific self-repair strategy was studied, the corresponding self-repair circuit fault system was designed, and the typical faults were simulated and analyzed which combined with the actual electronic devices. Simulation results demonstrated that the proposed fault self-repair strategy was feasible. Compared to traditional techniques, fault self-repair based on EHW consumes fewer hardware resources, and the scope of fault self-repair was expanded significantly.

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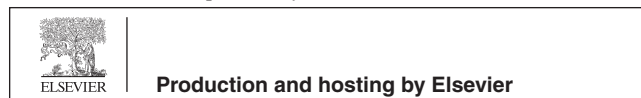
1. Introduction

With the development of the information technology and the electronic systems, which are mainly composed of large-scale integrated (LSI) and the very large scale integrated (VLSI) circuit with the field programmable gate array (FPGA) as their core component, are widely used in electronic equipments.^{1–4} Facing complex nature environment, such as dust, high and low temperature, strong electromagnetic scenes, the performance of digital integrated circuit in these electronic systems

^{*} Corresponding author. Tel.: +86 311 87994289.

E-mail address: cjyad@163.com (J. Cai).

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will be affected. The electronic systems will degrade, malfunction, or even cause significant casualties and property losses.¹⁻³

After being designed and produced, the traditional circuit structure of electronic equipment is fixed, and cannot be changed.¹⁻³ It is simple to implement the traditional redundant fault-tolerant technology based on fault self-repair technology, but the implementation cost is high and could not achieve redundancy backup for all plug-in or component level circuits, which limits its application in fault self-repair.⁵⁻⁷ It is very important to further improve the survivability of the electronic system in harsh environments, and ensure the digital system could work normally and lastingly.^{8,9} New methods of fault self-repair needs to be explored to solve these problems.

Based on evolvable hardware (EHW) and reparation balance technology (RBT), a new fault self-repair technology is proposed. The evolutionary algorithm (EA) is used as tool of combinational optimization and global search of EHW.¹⁰⁻¹² Through EHW evolves simulation expecting function of the circuit and the system structure, and makes full use of the advantages of the technique of EHW, such as robustness, self-organizing, self-adaptive.¹¹⁻¹⁵ By making full use of the fault signal, a correcting circuit through EHW technology is found to realize the balance of compensation of the fault signal output. This technology of fault self-repair strategy is different from the existing references.^{1,4,7,8,15} It can realize self-repair of multi-cell circuit fault dynamically, and is not limited to a certain kind of circuit.

2. Basic theory of EHW and RBT

2.1. Basic theory of EHW

EA is used as tool of combinational optimization and global search of EHW.^{11,14-16} The circuit and system structure can be obtained by simulating evolution.¹⁵⁻¹⁸ The chromosome coding of EAs are the structure of the programmable devices bit string, which can find better circuit structure.^{11,14,18-20} The evolution process is shown in Fig. 1.¹¹

EHW has a good feature of robustness, self-organizing and self-adaptive. Its formula is Evolutionary Algorithms + Programmable Logic Devices = Evolvable Hardware,^{10,11,18-20} that is $EAs + PLDs = EHW$.

In the field of fault self-repair, redundancy design is adopted to realize the fault self-repair in the existing references, while the application of fault self-repair based on EHW is absent.¹⁻³ Many references studied fault diagnosis technique and EHW separately, and their fusion applications failed to implement.^{10,14} Although some references used

EHW technique to realize fault self-repair, the fault self-repair mechanism was not researched clearly.²¹⁻²³

2.2. Basic theory of RBT

RBT is defined as follows. When the circuit output response is not consistent with the expected output, the original fault output-signals can be corrected through the additional rectification circuit (RTC) in output ports, so the expected output response can be obtained.

RTC is the abbreviation of rectification circuit. It can deal the fault signal directly, and it is the core of the RBT. The examples of RTC are shown in Section 3.2.

The fault self-repair strategy based on EHW and RBT include two parts: one part is state self-repair and the other is fault self-repair. This paper mainly studies the fault self-repair.

The evolved circuits have smaller scale at present, and the divide and rule technique is usually used in evolving large scale circuits. Its main idea is that the large scale circuits are decomposed into smaller circuit, and then the decomposed circuits are evolved. The problem of evolving large scale circuits has been the hot issue home and abroad. However, it is not the core of this paper.

3. RBT model and self-repair strategy analysis

3.1. RBT model

In order to analyze the fault self-repair strategy based on EHW and RBT effectively, it is necessary to model the self-repair fault. The response of normal circuit system is shown in Fig. 2(a), the equation $Y = X \bullet H(X)$ can be gotten. “ \bullet ” is an operator, but it is not limited to additional subtraction, multiplication and division, it usually includes AND, OR, NOT, XOR, and NOR of digital circuit.

After faults appear in the system response $H(X)$, the system response will be changed from $H(X)$ to $H_1(X)$. Here our concern is whether the fault exists or not, while the specific kind of the faults is not our concern. As shown in Fig. 2(b), when the output is changed from Y to Y_1 , Y_1 does not conform to the input-signal requirements of next level circuit. At this time, the fault system response $H_1(X)$ needs to be compensated and balanced. Through real-time detecting states, the faults characteristics can be recorded. According to these characteristics, the corresponding compensation balance circuit can be designed by EA, and the self-repair of fault circuit can be realized.

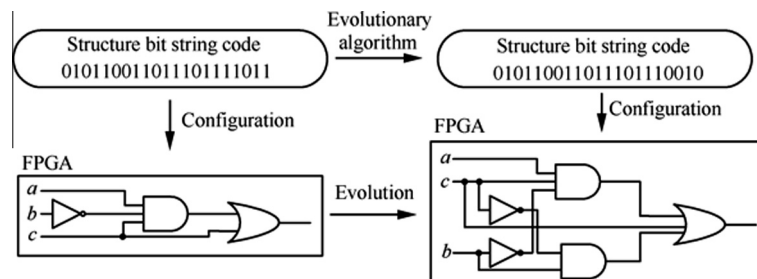


Fig. 1 Basic theory scheme of evolvable hardware.

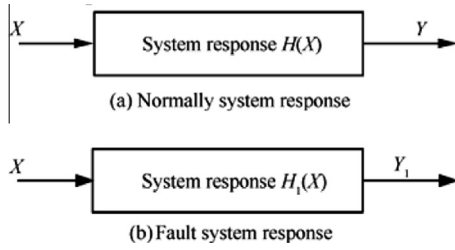


Fig. 2 Block diagram of two kinds of system responses.

The fault circuits are considered as black-boxes, only the inputs and outputs are concerned. If the inputs/outputs of working circuit are not consistent with the expectations, the fault can be judged. Here EHW is used in fault self-repair, which can take use of its self-organizing and self-adaptive characters.

According to the fault characteristics of the electronic circuit, the research on fault self-repair strategy based on EHW and RBT can be divided into two parts. One is joining the original input-states to guide the output fault signal to implement fault self-repair, the other is fault self-repair strategy regardless of the original input-states which means fault signal is processed directly at this time. Such as frequency division, filtering, shift, and so on. The principle block diagrams are shown in Fig. 3.

$H_0(X)$ is the system response of RTC. Fault self-repair associated with the input-states can be explained as follows. The fault output states can be divided by the input-states. X and Y_i are input to the offset balance circuit, so that the correct output Y can be obtained, the fault can be repaired. The scheme diagram is shown in Fig. 3(a).

Fault self-repair regardless of the input-states can be explained as follow. The input-states of X are not necessary to divide the fault output-states of Y_i . The fault can be repaired just by inputting Y_i to the offset balance circuit. The scheme diagram is shown in Fig. 3(b).

The difference between Fig. 3(a) and (b) is whether there is introduction of the original input X in the system response $H_0(X)$. The common target is achieving the fault system response output compensation balance, so that fault self-repair can be realized.

The Eqs. (1) and (2) can be gotten from Fig. 3(a) and (b).

$$Y = X \bullet H_i(X) \bullet H_0(X) \quad (1)$$

That is

$$H(X) = H_i(X) \bullet H_0(X) \quad (2)$$

The output response is still Y at this time.

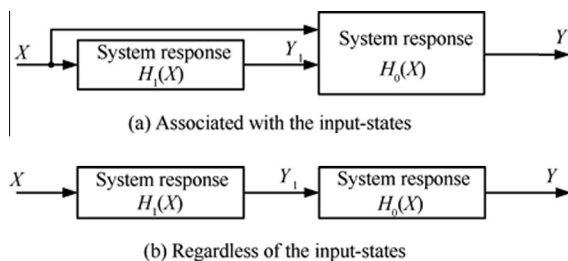


Fig. 3 Fault self-repair block diagram.

As for the first kind of fault self-repair strategy related to the input, signal “1” and “0” can be generated by n input signals. XOR operation can be executed between “0 or 1” and the original fault circuit output-signal, and the normal output can be gotten. Fault self-repair can be achieved by making full use of the Eq. (3). If a circuit contains n inputs, and $f(x_1, x_2, \dots, x_n)$ represents the corresponding output, the same conclusion will be gotten as follows.

$$\begin{cases} f(x_1, x_2, \dots, x_n) \otimes 0 = f(x_1, x_2, \dots, x_n) \\ f(x_1, x_2, \dots, x_n) \otimes 1 = \overline{f(x_1, x_2, \dots, x_n)} \end{cases} \quad (3)$$

where “ \otimes ” is exclusive-OR operator.

Using input signals can identify the time which output-signals needs to be balanced and compensated. The instance simulation will be analysis in Section 5.

For the second strategy of RBT fault self-repair based on regardless of input-states, when the system response is an electric wave signal, and a series jamming signal exists in a complex electromagnetic environment, the compensation circuit realized by RBT which is an adaptive filter. It can filter the interference signal, the normal signal can be obtained and fault self-repair can be realized. As compensation balance circuit does not introduce the original input-signals to confirm fault location, just related to the fault system output-signals. The instance simulation will be analyzed in Section 6.

3.2. RTC theory

The digital circuits can be divided into two parts, including combinational logic circuits and sequential circuits. Their fault self-repair technology based on EHW and RBT will be different, and the functions of RTC have small differences. Now the RTC theory will be explained as follows.

Example 1. Three-input majority voter is selected from combinational logic circuits. The truth table of fault circuit is shown in Table 1. When the input signals are “011” and “111”, the output signals are wrong.

According to the RBT model of Section 3.1, the RTC truth table can be obtained in Table 2 by using the Eq. (3). Fig. 4 is the RTC circuit. The simplification of Fig. 4 is shown in Fig. 5.

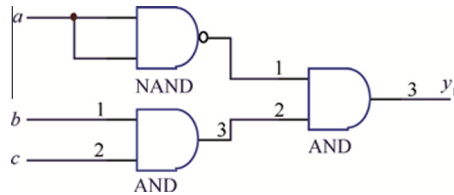
Fig. 6 has shown a complete fault self-repair circuit system. The RTC circuit is contained in RBT, in other words, $RTC + XOR = RBT$.

Table 1 Truth table of fault circuit.

Inputs			Output
a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table 2 Truth table of RTC.

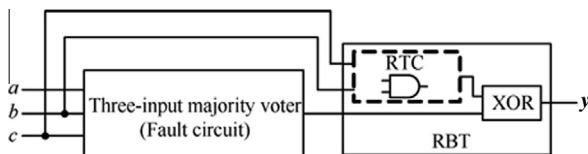
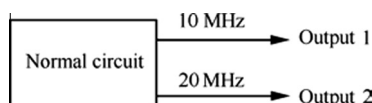
Inputs			Output
a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

**Fig. 4** RTC circuit.**Fig. 5** Best simple RTC of example.

Example 2. The RTC of some sequential circuits can also be used as [Example 1](#), and the RTC is parts of RBT. The sequential circuits have corresponding clock signals. When faults occurred in a sequential circuit, through the clock signal, corresponding fault output information and the Eq. (3), the RTC can be obtained.

The input-signals of RTC cannot be the fault circuit input-signals. They can be selected from the entire circuit system. However, the same sequence must be ensured.

However, another solution will be proposed when faults exist in some sequential circuits. The [Fig. 7](#) is an example for analysis. 10 MHz (Output 1) and 20 MHz (Output 2) signals can be produced when the circuit worked normally. When 10 MHz signal cannot be gotten, so fault is existed in circuit. At this time, 10 MHz signal can be obtained through

**Fig. 6** Fault self-repair circuit of [Example 1](#) based on RBT.**Fig. 7** Fault circuit of [Example 2](#).

frequency dividing 20 MHz signal under the condition of same sequential. The new obtained 10 MHz signal and the original signal must have same sequential.

[Fig. 8](#) is the complete fault self-repair circuit system. At this time, the RTC is a divider, and RBT is RTC. Compared with [Example 1](#), the XOR gate is not used.

The general conclusions can be stated as follows. For an n input ports m output ports combinational circuit, the fault input-output combinations needs to be confirmed beforehand. Next, the number of fault output ports should be confirmed, assuming its number is r ($1 \leq r \leq m$). Eventually, the corresponding RTC has n input ports and r output ports. The truth table has such characteristics, the output value of corresponding input combinations of fault circuit is 1, and other value is 0.

As sequential circuits have complex forms, the fault self-repair strategy based on EHW and RBT which is proposed in this paper has a limitation on scope. Different sequential circuits will have different RTC, for example, RTC can be as self-adaptive filter, an amplifier, a convolution, a frequency-divider and so on. If the self-repair target is frequency, RTC's function can be determined by the frequency division ratio. If the self-repair target is amplifying circuit, then RTC is a multiplication, and only the ratios needs to be compensated.

3.3. RBT based fault self-repair strategy analysis

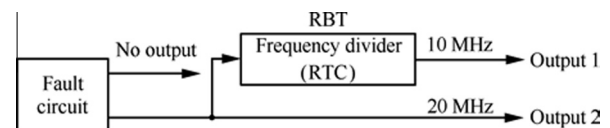
In order to balance the fault system response, the RTC needs to be found through EHW technique, and the release of the FPGA chip should evolve repairing function of the system response. The origin of the important parameters is guaranteed by EHW. At this time, EA can evolve whole original circuit function, and also can evolve the fault circuit important parameters.

[Fig. 9](#) is the fault self-repair universal model based on EHW and RBT. Circuit important node signals needs to be monitored at any time. In [Fig. 9](#), FPGA chips using as fault self-repair are embedded in the important nodes, so fault self-repair of the unit under test (UUT) can be achieved.

MUX_1 and MUX_2 have the following characteristics. MUX_1 can introduce input-signals to UUT and FPGA, and can be arbitrarily on and off. MUX_2 can introduce all the output-signals of the UUT to the FPGA, and introduces the FPGA output-signals to next level circuit, and can be arbitrarily on and off as well. Normally, the input-signals are input UUT directly by MUX_1 , the output-signals of UUT is sent to next level circuit by MUX_2 , the FPGA does not connect to the entire circuit.

If the troubleshooting signal is a digital signal, it can be directly connected to the FPGA chip. If the troubleshooting fault signal is an analog signal, the A/D and D/A conversion circuit are needed. The chip cannot be damaged.

EHW have two ways, including internal evolution and external evolution. In this paper, the later is selected in the EHW process.^{6,10,13–16}

**Fig. 8** Fault self-repair circuit of [Example 2](#) based on RBT.

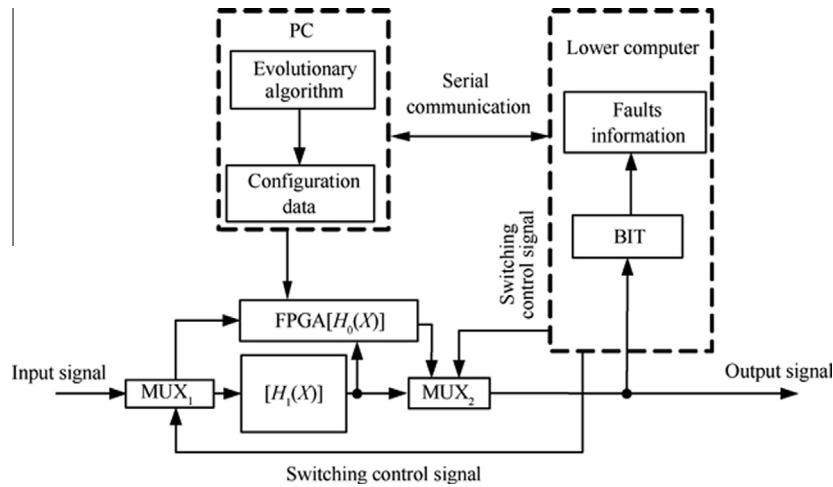


Fig. 9 Universal model of fault self-repair based on RBT.

The basic steps of fault self-repair based on EHW and RBT in Fig. 9 are as follows:

Step 1. The UUT circuit is detected by built-in test (BIT) circuits, and is diagnosed. If faults are not founded in the UUT, in addition to continue BIT detection, other operation does not needs to do. If faults are founded in the UUT, the faults information must be stored, BIT detection must be executed, and Step 2 is executed.

Step 2. Faults information is be sent to PC by serial communication, and then the EA program should be started by control system of PC.

Step 3. External evolution is selected, and genetic algorithm particle swarm optimization (GAPSO) is used.^{23–27} The GAPSO operations are executed in EA, the individuals are evaluated later.^{23–27} Repeat the above steps until the EA stop conditions are satisfied. The optimum codes are sent to FPGA by serial communication, FPGA is configured by them. If evolution has reached the maximum number of iterations and it has not found the optimal circuit coding, fault self-repair is announced failure.

Step 4. PC send the control data of MUX to the Lower Computer by serial communication based on the fact self-repair strategy. The MUX control instructions are executed by lower computer, and MUX is controlled by lower computer.

3.4. Advantages of proposed fault self-repair strategy

The EHW and RBT fault self-repair strategy proposed in this paper is different from traditional technique based on EHW. The former just need evolve and repair the fault output-signals instead of the whole fault circuit, while the latter needs to evolve whole circuit.

On this basis, the evolution of the former circuit will be smaller than the later. The rate of evolved circuit will be directly affected by the scale of evolved circuit. If the evolved circuit has greater scale, the number of evolution iterations will be larger, and time will be longer.

The traditional fault self-repair method based on redundant fault-tolerant technology is simple to implement, but

the cost is high. The method cannot be used in all plug-in or component-level circuits to realize redundant backup, which limits its application in self-repair. For example, triple modular redundancy (TMR) is a traditional and classic redundant fault-tolerant technology. If TMR is used in all components of an electronic system, the hardware cost will be increased. The weight and volume of electronic system will be changed, which can directly affect and even limit the use of electronic systems in some special environment.

Disadvantages above can be avoided by a novel fault self-repair strategy proposed in this paper. Multiple UUTs can be repaired by a same FPGA fabric, and different RTC can be realized within one region of the reconfigurable fabric. In other words, many redundancies based on TMR can be replaced by amorphous PFPGA resources. MUXs can be designed in multiple circuit nodes, any digital signal can be input FPGA through MUX. Multiple different fault signals can be repaired by FPGA through using EHW and RBT.

The proposed fault self-repair strategy has adopted integrated design. The strategy needs to satisfy the circuit function and self-repair ability. At the same time, signal access is realized without interference through the MUX. The system will be degraded when faults occur in the UUT. Yet ideally, normal throughput will not be affected by the self-repair process. An evolved circuit is configured on FPGA fabric, and the core function is a MUX.

The reliability of the electronic system mainly includes the durability, maintainability and reliability design.^{28,29} The redundancy provision of conventional techniques relies on spatial redundancy, such as TMR is realized by using the same circuit module at design-time. In contrast, the proposed fault self-repair circuit system based on EHW and RBT belongs to a category of run-time evolutionary approaches in the series system. So the long term sustainability can be less than the traditional one.

However, the core component of the fault self-repair strategy proposed is FPGA, it has very high reliability. FPGA is used as redundant hardware, and is also referred to as the hardware platform of EHW. Thus the reliability of the entire circuit system has been a little affected. The proposed self-repair circuit is a new circuit design concept,

and it is able to reduce the burden of fault repair afterwards. FPGA devices must go through production test before leaving the factory, which includes whole nodes test and 2000–3000 times configured program test. The overheating capability of FPGA can be less than application specific integrated circuit (ASIC), so FPGA can be sought for high reliability in complex harsh environment, such as universe, abysmal sea and so on.

Of course, many research institutions are researching a novel bionic hardware, which is more suitable for EHW. Their reliability indexes will be strictly considered in the process of designing novel bionic hardware.

The durability of proposed fault self-repair system is enabled by the high reliability of FPGA fabrics. The availability and maintainability of proposed fault self-repair strategy are verified in Sections 5 and 6. It should be noted that the use of FPGA may help improve the reliability of electronic systems, especially for optimizing evolutionary circuits. As to the circuit system, its normal work cannot be affected by burrs and other adverse factors, and these problems can be avoided by EA.

Because TMR has three identical redundant modules, they are prone to so-called common mode failures (CMF) under the condition of the same interference at the same time, and CMF is addressed in many references. For TMR design, once the circuit structure is fixed, the design cannot be changed. This is their biggest weakness. However, in this paper, the proposed fault self-repair strategy can overcome this shortcoming, which can directly repair the fault signal based on RBT. Using the technique of EHW can adaptively change the structure of RTC. For this reason, the adaptability of proposed fault self-repair strategy will be more sustainable to multiple faults than traditional spatial redundancy designs.

4. Scopes of fault self-repair strategy based on EHW and RBT

Any method and theory has its applicable scope. The applicable scopes of fault self-repair strategy based on EHW and RBT are analyzed in this section.

In theory the following circuits can realize fault self-repair based on EHW and RBT. Such as combinational circuits, frequency division circuits, frequency multiplication circuits, amplifying circuits, attenuation circuits, FFT computation, filter and convolution.

Because of the limited capability and parameter restrictions of FPGA, if RTC can be implemented in FPGA, faults can be repaired in theory.

5. Instance simulation of fault self-repair associated with the input-states based on EHW and RBT

5.1. Typical fault analyzed

Fig. 10 is the signal processing circuit of electronic system, and it contains a 2-bit adder. Fig. 11 is adder fault self-repair circuit system design chart based on EHW and RBT.

In the process of working circuit, fault information is found by BIT. When the inputs combination ($A_1, A_2, B_1, B_2, c_{in}$) are 01001, the outputs combination (C_1, C_2) are 11, but the correct outputs are 10. The fault only exists in C_2 .

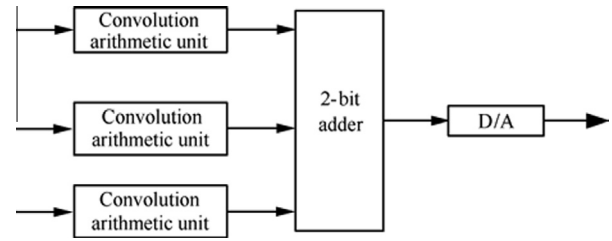


Fig. 10 Signal processing circuit of electronic system.

Adder circuit is integrated by a chip, and its output port C_1 is wrapped with C_2 . If the original adder is evolved circuit, it will spend much time. When the 2-bit adder is analyzed in detail, we can find that the C_1 and C_2 side are independent outputs. Output C_2 will not be any affected by the output C_1 . So the C_1 column can be removed from evolved circuit truth table. After the C_1 column is deleted, the evolved truth table size will be halved, and the convergence of the evolution speed can be significantly accelerated.

The fault self-repair technology based on EHW and RBT will be compared with the traditional fault self-repair technology based on EHW. The comparison of the simulation results will be shown in Section 5.2.

5.2. Simulation experiment

In the simulation experiment, ternary chromosome coding scheme is selected, 4×5 matrix is used as encoding size scale. Genetic algorithm particle swarm optimization (GAPSO) is as EA. Because the EA is not focused in this paper, GAPSO is not researched in details.

In EA, the number of initial samples are $N = 40$, crossover rate is $pc = 0.95$, mutation rate is $pd = 0.05$, crossover operator uses 2-points crossover, mutation operator uses 2-points mutation. The inertia weight of GAPSO is expressed by Eq. (4).

$$w = 0.9 - \frac{0.4t}{t_{\max}} \quad (4)$$

where t is current iteration numbers, t_{\max} is maximum iteration numbers. The best fitness function is Eq. (5).

$$\text{fitvalue} = \sum_{i=1}^{2^n} \text{fitnumber}_i \quad (5)$$

where fitvalue is best fitness function, i is input combination number of truth table ($i \in [1, 2^n]$), fitnumber_i is test value of i th input combination ($\text{fitnumber}_i \in \{0, 1\}$).

The best fitness is $\text{fitvalue} = 32$. 50000 times are set as the maximum number of iterations (if the number of iteration are set too large, evolution time would be extended directly). If 50000 times are reached, and the fitness cannot be found, evolution circuit failure can be declared.

Optimize strategy must be always used in EA, which means that the logical unit consumption should maintain least level to save hardware resource.

The results of the simulation experiment are shown in Fig. 12. Evolvable iteration times are 8712 when evolved circuit is original adder. However, when evolved circuit is RTC, evolvable iteration times are 3298. The best fitness value, also

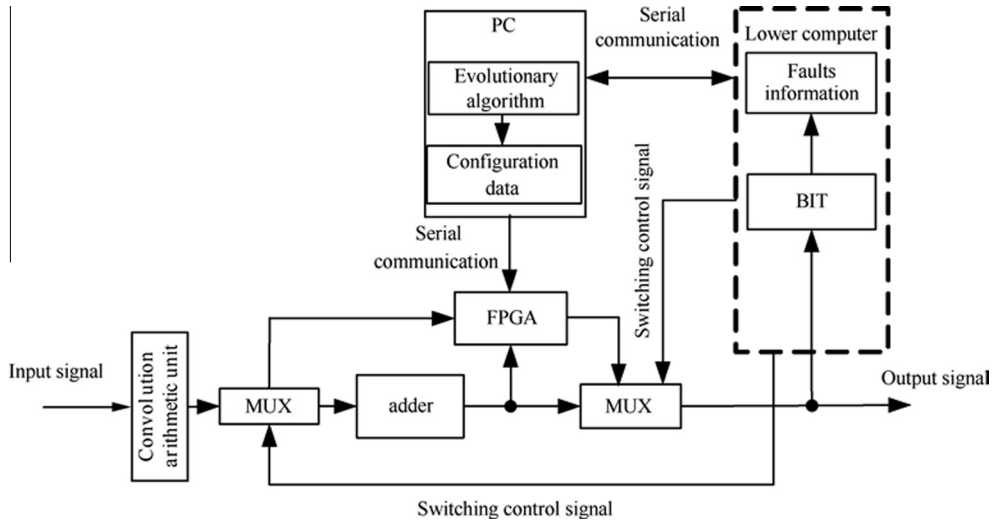


Fig. 11 Adder fault self-repair circuit system design.

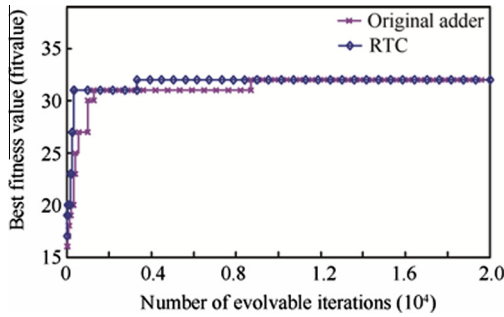


Fig. 12 Two evolution iteration times contrast diagram of the circuit.

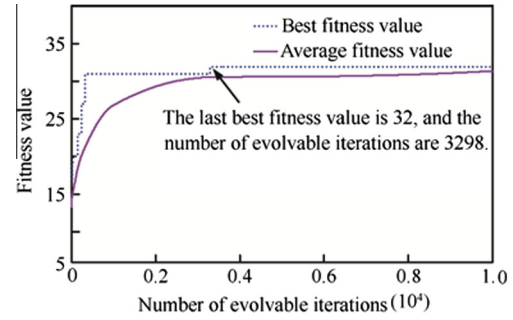


Fig. 13 Relationship between best fitness value and average fitness value.

the optimal value, is gotten. That is, $\text{fitvalue} = 32$. The numbers of iterations of comparative experiments are within 50000 times, which meet the requirements of the success evolution.

The results of the simulation experiment show that the RTC evolved is better than the original adder evolved. The convergence can be achieved rapidly, target circuit can be found and fault self-repair can be realized. The main reason is that truth table scale of adder is twice the size of RTC in the process of evolution computation. Because GAPSO is adopted, the best fitness value reaches $\text{fitvalue} = 31$ soon. But in the end, from 31 to 32, the original adder need more than 6000 times iterative evolution, but the RTC only need about 2000 times iterative evolution.

In the process of evolving circuit, the differences between best fitness value and average fitness value are researched. Here the RTC evolved is taken as an example. The performance of GAPSO is reflected in Fig. 13. Average fitness value rises quickly before 850 generations. The rising speed of average fitness value is reduced, and the rising tend becomes very slow in 3000 generations. However, it is monotonically increasing, and it has been close to last best fitness value. Moreover, the best fitness value reaches 31 in 324th generation. But the last best fitness value is obtained in 3298th generation, and it is 32.

After evolution convergence speed is judged, hardware resource consumption will be analyzed. Xilinx ISE Design Suite 12.2 is adopted, the chip model is 3s250etq144-5, and the comparing results are shown in Table 3. We can see clearly from the Table 3, hardware resources of RTC are saved than original adder, which is mainly reflected in the assessment of input output block (IOB), look-up-table (LUT) and Slice.

Finally, the best encoding matrix is shown below

$$E = \begin{bmatrix} 2 & 2 & 2 & 2 & 2 \\ 0 & 1 & 0 & 0 & 1 \\ 2 & 2 & 2 & 2 & 2 \\ 2 & 2 & 2 & 2 & 2 \end{bmatrix} \quad (6)$$

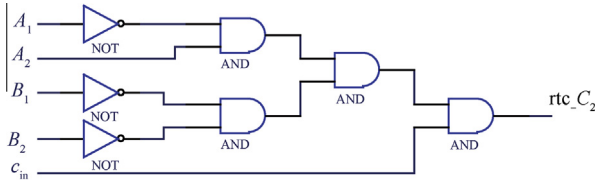
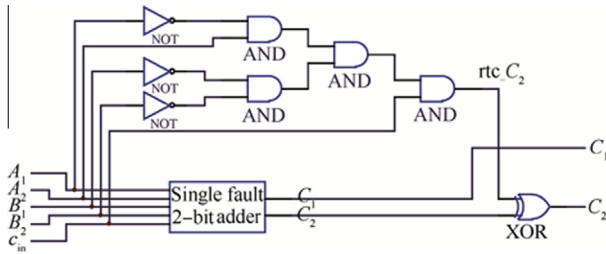
The corresponding binary fixed-length chromosome encoding is: 0000000000001100101100000000000000000000. The evolution of its corresponding circuit (RTC) is shown in Fig. 14.

The RTC should integrate into the original fault circuit based on RBT, so that RBT circuit system can be formed. Fig. 15 is the RBT circuit system, the fault output C_2 can be self-repaired through the RTC, and the correct output-signals can be gotten.

Fig. 16 is the RBT circuit system function simulation waveform of 2-bit adder with single fault, we can get conclusion

Table 3 Table of hardware resource impropriation for two kinds evolvable circuits.

Parameter	Evolvable ways	Used	Available	Utilization (%)
Number of slices	Original adder	3	2448	0.1
	RTC	1	2448	0
Number of 4 input LUTs	Original adder	5	4896	0.1
	RTC	1	4896	0
Number of bonded IOBs	Original adder	7	108	6.5
	RTC	6	108	5.5

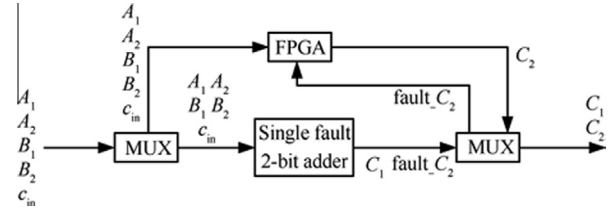
**Fig. 14** Result of evolution RTC.**Fig. 15** RBT circuit system of 2-bit Adder with single fault.

clearly as follows from the figure. Only when the input signal ($A_1, A_2, B_1, B_2, c_{in}$) is 01001, the rtc_C_2 is “1”, the rest time is “0”. rbc_C_2 and $fault_C_2$ have opposite level only. In other words, $fault_C_2 = 0, rbt_C_2 = 1$. Through the Eq. (3), Eq. (7) can be gotten as follows.

Where rtc_C_2 is output signal of RTC, and it is rtc_C_2 of Fig. 15. rbc_C_2 is output signal of RBT, and it is C_2 of Fig. 15. $fault_C_2$ is fault circuit output signal.

$$rbt_C_2 = fault_C_2 \otimes rtc_C_2 \quad (7)$$

Because RBT circuit system model is adopted at this time, the Eq. (7) is used, rbt_C_2 is 1, and the output of the result is constant “1”. The paths of fault self-repair circuit signal flows are shown in Fig. 17.

**Fig. 17** Path of fault self-repair circuit signal flow.

Through the analysis of the function simulation diagram, the effectiveness and superiority of fault self-repair based on EHW and RBT is proved.

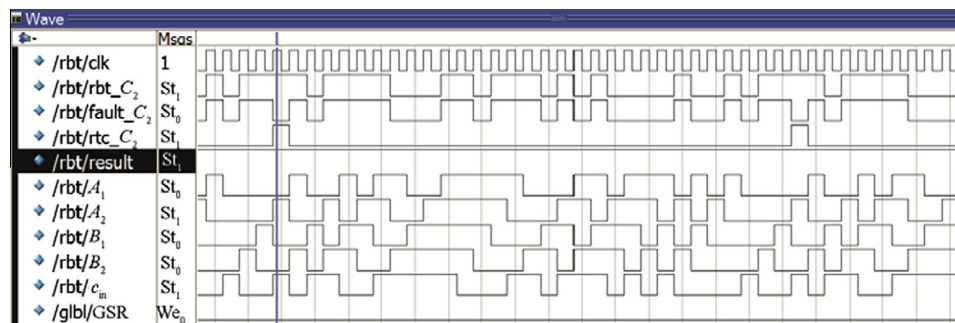
When faced with multiple faults, the fault self-repair strategy based on EHW and RBT is still valid. Only the size of the code needs to be increased, the EA convergence speed will be affected directly by the increasing code size.

6. Instance simulation of fault self-repair regardless of input-states based on EHW and RBT

Not all faults in electronic system can be repaired by introducing input-states by using the Eq. (3). For example, when the electronic systems are affected by complex electromagnetic environment, the interference signal is stringed into signal path, or the signal amplitude becomes lower or higher, or the analog signal phase is not correct, or the output signal frequency is not accurate, and so on. These faults can be self-repaired by using the irrelevant input-states fault self-repair strategy.

6.1. Typical fault analysis

In a complex electronic device, there are multiple clock signals when it works normally. The major clock signals are 12, 6 and 0.6 MHz, which are got by reshaping and frequency dividing.

**Fig. 16** RBT circuit system function simulation waveform of 2-bit adder with single fault.

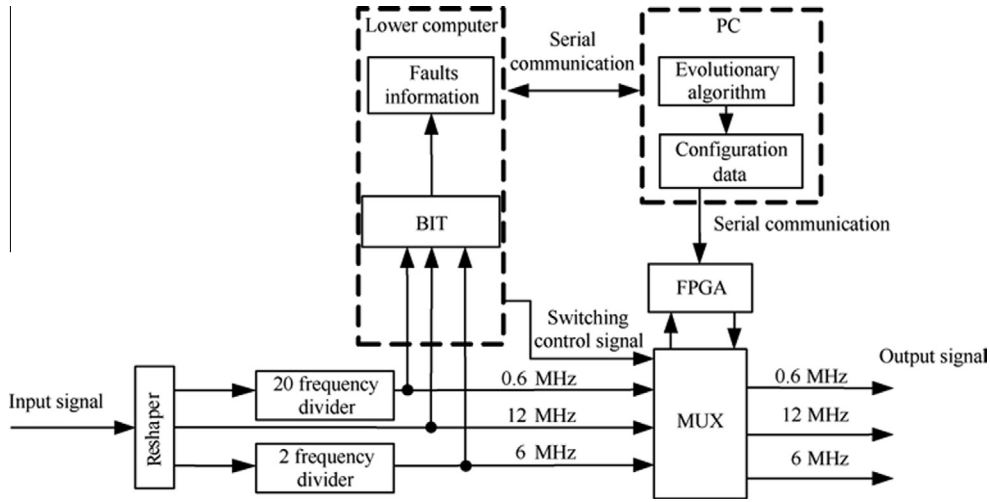


Fig. 18 Clock signal circuit fault self-repair circuit system design chart.

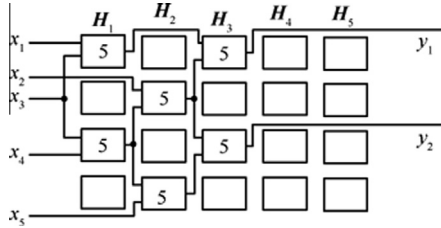


Fig. 19 Circuit configuration of C_{17} .

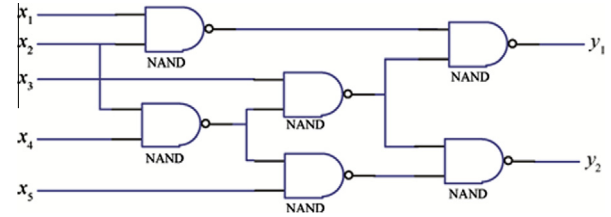


Fig. 20 Circuit of C_{17} .

Fig. 18 is design chart of fault self-repair circuit system for the clock signal circuit. All three clock signals are tested by BIT. By counting the clock pulses and comparing the count result with truth value, it can determine whether faults are existed.

0.6, 6 and 12 MHz clock signals are generated from the same complex programmable logic device (CPLD) chip, which may appear various faults. There is a case when 0.6 MHz clock signal can't be counted correctly, but 6 and 12 MHz clock signals are normal. The reason may be that CPLD logic units are affected by ray, or 0.6 MHz clock signal output pin appears virtual weld.

6.2. Encoding strategy and the selection of EA

LUT is look-up-table, it is important component of FPGA. Arbitrary 4-input circuits can be realized by a LUT. In order to demonstrate encode strategy visually, the 4-input LUT is replaced by 2-input LUT, as it shows in Fig. 19. Taking C_{17} of ISCAS '85 standard circuit is as an example, and Fig. 20 is the circuit of C_{17} .

Each logical block is designed to realize 2-input-1-output logic. All possible combinations of two inputs needs to be encoded. Here the decimal coding is adopted, and the encoding results are shown in Table 4. Therein the logical block without any function is respected by NULL.

There are five coordinate codes in the logical block. The first and second coordinate codes represent the first input, while the second input is represented by third and forth coordinate codes. Logic is represented by the fifth coordinate code.

Table 4 Code table of basic logic units.

Logic	Code
AND	1
OR	2
NOT	3
XOR	4
NAND	5
XNOR	6
NOR	7
D Flip-flop	8
NULL	0

For example, module of second row second column is encoded in Fig. 19. It has two input ports. The first input -signal comes from first row second column output-signal, so the code is "12". The second input-signal comes from the output signal of second row third column, so the code is "23". Because this module's function is NAND, so the code is "5", it can be referred in Table 4. So this module's code is "12235".

Each module is encoded in the same way, each column module code forms a matrix codes, examples will be shown as follows.

Fault self-repair has to abide the following rules.

Definition 1. The unused module is dormancy module (redundant module).

Since dormancy modules have not been applied, the logic code is "0". Two inputs have no input-signals, so the

inputs-signal coordinate codes are “0000”. The final dormancy module code is 00000.

Definition 2. Every column is treated as a layer, and the input layer is not included in the logic array code. H_j is $j + 1$ th layer code. The original input-signal is first layer code. For example, the logic array scale of Fig. 19 is 4×5 , it has a total of five layers, which are shown as follows:

$$H_1 = \begin{bmatrix} 1 & 1 & 1 & 3 & 5 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 3 & 1 & 4 & 5 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, H_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 2 & 2 & 3 & 5 \\ 0 & 0 & 0 & 0 & 0 \\ 2 & 3 & 1 & 5 & 5 \end{bmatrix},$$

$$H_3 = \begin{bmatrix} 2 & 1 & 3 & 2 & 5 \\ 0 & 0 & 0 & 0 & 0 \\ 3 & 2 & 3 & 4 & 5 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, H_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$H_5 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Definition 3. If the input coordinates do not exist in upper layer, it is an illegal individual. Because the goal of evolution circuit belongs to sequential circuits, $(u + \lambda) - ES$ is adopted. Since it is a relatively mature study,³⁰ this paper does not study it in detail.

6.3. Simulation experiment

Here we assume there is a fault in 0.6 MHz clock signal, and it has been detected by BIT. The preferred solution is that 6 MHz is divided by two-frequency-divider. At this time, the size of the chromosome initialization is: $3 \times 5 \times 12 \times 6$, $3 \times 5 \times 12$ is a chromosome code, u is 6, λ is 4, so $u + \lambda = 10$. Where u is the number of parent-individual, λ is the number of offspring-individual.

Fixed mutation rate $pd = 0.05$ is used in $(u + \lambda) - ES$, the illegal mutated individuals must be cleared in the variation process.

Evolved circuit function verification is required in the process of EHW, the available logical unit must be counted, and the purpose is to make use of minimum hardware resource consumption. The evolution experiments are carried out eight times under the same conditions, evolution results are shown in Table 5.

The average number of iterations of eight experiments are 253 times, the optimal target circuit evolved (less hardware resources) only uses one gate and five D Flip-flops. Three

Table 5 Statistics of the evolution results of 10-frequency-divider.

Serial number	Number of evolution iterations	D Flip-flop used	Number of basic logic unit used	Slices used
1	253	5	1	3
2	262	6	3	3
3	243	5	5	3
4	249	8	1	4
5	271	5	3	3
6	239	9	2	4
7	242	11	3	6
8	265	7	5	4

Table 6 Hardware consumption of 10 division frequency divider.

Parameter	Used	Available
Number of Slices	3	2448
Number of Slice flip flops	5	4896
Number of 4 input LUTs	1	4896
Number of bonded IOBs	2	108

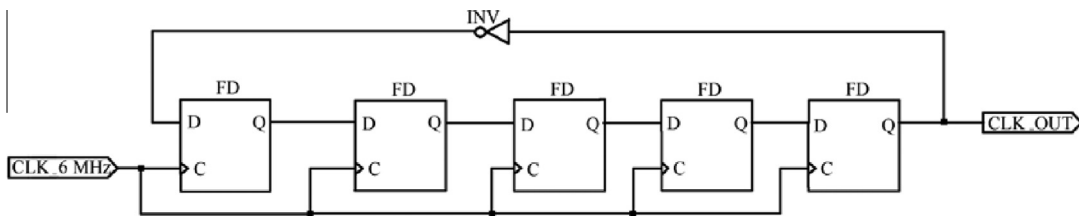


Fig. 21 Target circuit evolved.

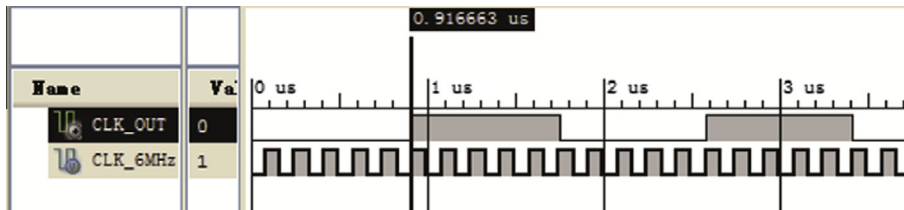


Figure 22 Function simulation figure of 10 division frequency-divider.

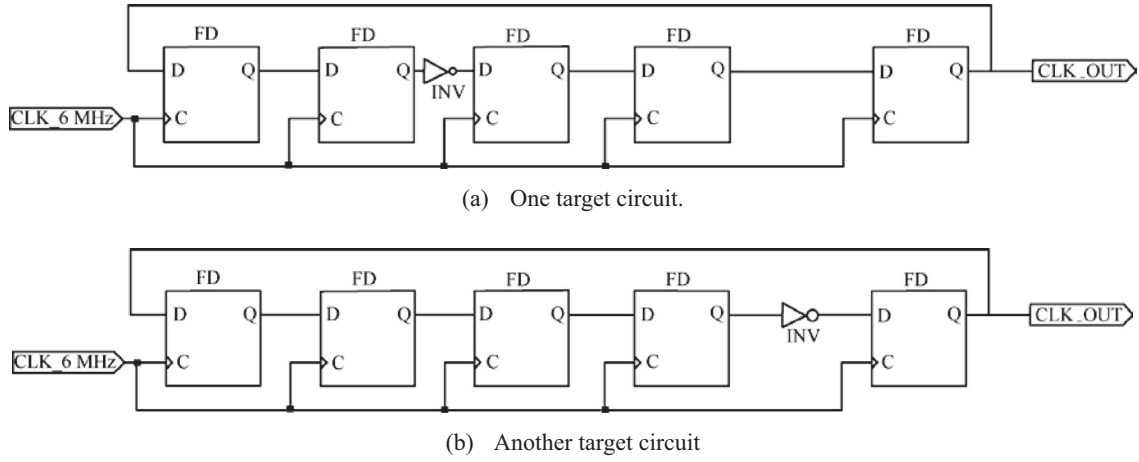


Fig. 23 Two kinds target circuit meeting the requirements.

Slices of the FPGA are used, with a range from 6th layer to 12th, the corresponding code are shown as follows:

$$H_6 = H_7 = H_8 = H_9 = H_{10} = H_{11} = H_{12} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Codes from the first to the fifth layer are arranged as follows:

$$H_1 = \begin{bmatrix} 2 & 2 & 1 & 1 & 8 \\ 6 & 1 & 0 & 0 & 3 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, H_2 = \begin{bmatrix} 2 & 1 & 1 & 1 & 8 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$H_3 = \begin{bmatrix} 3 & 1 & 1 & 1 & 8 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, H_4 = \begin{bmatrix} 4 & 1 & 1 & 1 & 8 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$H_5 = \begin{bmatrix} 5 & 1 & 1 & 1 & 8 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The above optimal circuit code is decoded, and the actual circuit can be gotten in Fig. 21.

The function simulation of above circuit is shown in Fig. 22. 6 MHz clock signal period is 0.167 μ s, which is processed by the evolved circuit. We can see from Fig. 22, the output electronic level is reversed after five rising edges. The results have been repeated. CLK_6 MHz clock signal is divided into CLK_OUT signal, the periodic of CLK_OUT signal is 1.67 μ s.

Five D flip-flops and one gate are used in 10-frequency-divider, and two IOB ports are used. The detailed hardware resources consumption is shown in Table 6.

Through evolution, there are many target circuit can be found without restricted condition of least hardware resources. The circuit will still be more than one, but they have different circuit codes. Although these circuits have different structures, they can accomplish the same function and consume equal hardware resources.

Fig. 23 also show two different target circuits which also meet the requirements.

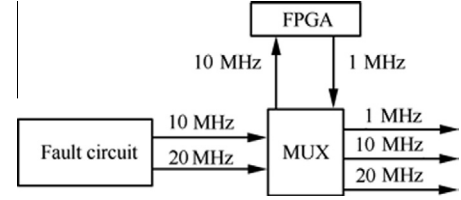


Fig. 24 Path of fault self-repair circuit signal flow.

The paths of fault self-repair circuit signal flows are shown in Fig. 24.

After the above evolution process, we can get a 10-frequency-divider circuit, which can realize the frequency division of 6 MHz clock signal, and get 0.6 MHz clock signal. Fault self-repair have been realized. The feasibility of fault self-repair strategy based on EHW and RBT is proved. The general fault self-repair scopes based on EHW are expanded. It has important value of engineering application.

7. Conclusions

- (1) Compared with the general fault self-repair technology based on redundant fault-tolerant and EHW technology, a new fault self-repair strategy based on EHW and RBT was proposed in this paper. When this technology is used, there is not need to evolve the whole fault circuit, and only a RTC needed to be designed, and the fault signal can be balanced and the target output signal can be obtained.
- (2) The general model of proposed fault self-repair strategy based on EHW and RBT was analyzed, the fault self-repair circuit system is designed, and the application scopes of the strategy are analyzed. Through typical faults simulation experiments, the feasibility and superiority of the proposed fault self-repair evolution strategy are proved.
- (3) The proposed fault self-repair strategy can reduce the hardware resources consumption shorten the fault self-repair time, and expand the scopes of fault self-repair.

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Zhang Junbin is a Ph.D. student at Department of Electronic and Optical Engineering, Mechanical Engineering College. He received his B.S. degree from University of Electronic Science and Technology of China, and received his M.S. degree from Mechanical Engineering College. His research interest is evolvable hardware and fault self-repair of electronic systems.

Cai Jinyan is a professor and Ph.D. supervisor. She received B.S. degree from Nanjing University of Science and Technology, she received M.S. degree from Tsinghua University and received Ph.D. from Nanjing University of Science and Technology. Her area of research includes electronic system fault diagnosis, electronic system reliability, fault self-repair and evolvable hardware.

Meng Yafeng is an associate professor and Master supervisor at Mechanical Engineering College. She received his B.S., M.S. degrees and Ph.D. from Mechanical Engineering College. His area of research includes electronic system fault diagnosis, electronic system reliability.